REMARKS

Claims 29-45 are all the claims presently pending in the application. Claims 24-28 have been canceled and claims 29-45 have been added to claim additional features of the invention.

It is noted that the claim Amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability.

Claims 24-28 stood rejected under 35 U.S.C. § 103(a) as being unpatentable over either one of Witek et al. (U.S. Pat. 6,146,970), or Chen et al. (U.S. Pat. 5,767,549) or Tsuchiaki (U.S. Pat. 6,051,509).

These rejections are respectfully traversed in view of the following discussion.

I. THE CLAIMED INVENTION

The claimed invention is directed to a semiconductor device having a bulk silicon region, and a silicon-on-insulator (SOI) region. Further, the SOI region has a crystallized silicon layer formed by annealing amorphous silicon and having isolation trenches formed therein so as to remove defective regions, and isolation oxides formed in the isolation trenches.

Conventional substrates are formed of either SOI regions or bulk silicon regions. However, it is desirable to include different devices on the substrate, some of which are preferably formed on bulk silicon, and some of which are preferably formed on SOI. Therefore, if both types of these devices are formed on one substrate (e.g., bulk silicon), some performance sacrificed with respect to the type of device preferring the other substrate (e.g., SOI).

The claimed device, on the other hand, has a hybrid bulk silicon and SOI substrate. Specifically, the substrate in the claimed invention has an SOI region with a crystallized silicon layer formed by annealing amorphous silicon and having isolation trenches formed therein so as to remove defective regions. Therefore, unlike conventional devices, the claimed device can efficiently accommodate both devices preferably formed on SOI and

devices preferably formed on bulk silicon.

II. THE PRIOR ART REFERENCES

A. The Witek Reference

The Examiner alleges that Witek discloses the claimed method. Applicant submits, however, that there are elements of the claimed method which are neither taught nor suggested by Witek.

Witek discloses a method of forming a capped shallow trench isolation which includes forming a trench region within a substrate, depositing a first trench fill material within the trench region after forming a first liner region, removing a portion of the first trench fill material to form a first trench plug region within the trench region, removing a portion of the first trench fill material to form a first trench plug region within the trench region, removing a portion of the first liner region to expose a portion of the substrate, depositing a second trench fill material overlying the first trench plug region, and removing a portion of the second trench fill material to form a second trench plug region (Witek at col. 11, lines 25-49).

However, Witek does not teach or suggest "a crystallized silicon layer formed by annealing amorphous silicon and having isolation trenches formed therein so as to remove defective regions" as recited in claim 29. As explained in the Application, many devices cannot be formed in an SOI substrate (Application at page 2, lines 3-4). Therefore, conventional semiconductor devices are often formed on one of either SOI substrate or bulk silicon substrate (Application at page 2, lines 2-10). However, some devices are not easily formed on SOI substrates and, moreover, some devices are preferably formed on bulk silicon and some devices are preferably formed on SOI substrate (Application at page 2, lines 14-20). Therefore, if both types of these devices are formed on one substrate (e.g., bulk silicon), some performance sacrificed with respect to the type of device preferring the other substrate (e.g., SOI).

The claimed device, on the other hand, has a hybrid bulk silicon and SOI substrate (Application at page 6, line 19-page 7, line 3; Figure 2G). Specifically, the SOI portion of the claimed device includes a crystallized silicon layer formed by annealing amorphous silicon

and having isolation trenches formed therein so as to remove defective regions (Application at page 9, lines 4-11; Figures 1D and 2C-2F). Therefore, unlike conventional devices, the claimed device can efficiently accommodate devices preferably formed on SOI (e.g., high speed or noise-sensitive circuits, such as DRAM arrays) as well as devices preferably formed on bulk silicon (e.g., temperature-sensitive circuits such as logic devices).

Witek, on the other hand, does not teach or suggest these novel features. Indeed, nowhere does Witek disclose a crystalline silicon layer formed by annealing an amorphous silicon layer, let alone isolation trenches formed in the defective regions of the crystalline silicon layer. Witek merely states that the polysilicon layer 206 "may be replaced by other materials such as amorphous silicon" (Witek at col. 6, lines 24-25). However, Applicant notes that layer 206 is not even in a SOI region. Note, for instance, that layer 206 is formed over bulk silicon 202, not over an insulator layer.

Therefore, Applicant submits that Witek does not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

B. The Chen Reference

The Examiner alleges that Chen discloses the claimed method. Applicant submits, however, that there are elements of the claimed method which are neither taught nor suggested by Chen.

Chen discloses a silicon-on-insulator (SOI) CMOS structure which is intended to overcome floating gate problems caused by charge accumulation below the channel of metal oxide semiconductor field effect transistors (MOSFETs). The Chen device includes a substrate, a layer of insulator, a layer of silicon having raised mesas and thin regions therebetween to provide ohmic conduction between mesas, electronic devices on the mesas, and interconnection wiring (Chen at Abstract).

However, Chen, like Witek, does not teach or suggest "a crystallized silicon layer formed by annealing amorphous silicon and having isolation trenches formed therein so as to remove defective regions" as recited in claim 29. As explained above, conventional devices do not have efficiently formed combination SOI and bulk silicon substrates (Application at

page 2, lines 3-4). Therefore, devices are often formed on one of either SOI substrate or bulk silicon substrate (Application at page 2, lines 2-10).

The claimed device, on the other hand, has a hybrid bulk silicon and SOI substrate (Application at page 6, line 19-page 7, line 3; Figure 2G). Therefore, unlike conventional devices, the claimed device can efficiently accommodate devices preferably formed on SOI (e.g., high speed or noise-sensitive circuits, such as DRAM arrays) as well as devices preferably formed on bulk silicon (e.g., temperature-sensitive circuits such as logic devices).

Chen, on the other hand, does not teach or suggest these novel features. Indeed, like Witek, nowhere does Chen disclose a crystalline silicon layer formed by annealing an amorphous silicon layer, let alone isolation trenches formed in the defective regions of the crystalline silicon layer. Chen merely discloses "[a] layer of single crystal semiconductor material 18 such as silicon, SiGe, SiC or GaAs ... positioned on upper surface 15 of layer of dielectric material 14" (Chen at col. 2, lines 64-67; Figure 1). However, Chen does not even disclose a combination bulk silicon and SOI substrate let alone, a hybrid substrate having a SOI region as in the claimed invention. For instance, Chen does not even disclose defective areas of a crystalline silicon layer, let alone removing defective regions to form isolation trenches.

Therefore, Applicant submits that Chen does not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

C. The Tsuchiaki Reference

The Examiner alleges that Tsuchuiaki discloses the claimed method. Applicant submits, however, that there are elements of the claimed method which are neither taught nor suggested by Tsuchiaki.

Tsuchiaki discloses a method of forming an integrated circuit device which includes forming a first carbon-containing semiconductor layer in a first region on a surface of a semiconductor substrate, forming a second carbon-containing semiconductor layer in a second region on the surface, and forming first and second gate-insulation layers in the first and second carbon-containing semiconductor layer, each gate-insulation layer having a film

thickness dependent on the carbon content in the corresponding carbon-containing semiconductor layer (Tsuchiaki at col. 21, line 64-col. 65, line 10).

However, Tsuchiaki, like Chen and Witek, does not teach or suggest "a crystallized silicon layer formed by annealing amorphous silicon and having isolation trenches formed therein so as to remove defective regions" as recited in claim 29. As explained above, conventional devices are often formed on one of either SOI substrate or bulk silicon substrate (Application at page 2, lines 2-10). The claimed device, however, has a hybrid bulk silicon and SOI substrate (Application at page 6, line 19-page 7, line 3; Figure 2G). Therefore, unlike conventional devices, the claimed device can efficiently accommodate devices preferably formed on SOI (e.g., high speed or noise-sensitive circuits, such as DRAM arrays) as well as devices preferably formed on bulk silicon (e.g., temperature-sensitive circuits such as logic devices).

Tsuchiaki, on the other hand, does not teach or suggest these novel features. Indeed, nowhere does Tsuchiaki teach or suggest isolation trenches formed in the defective regions of a crystalline silicon layer. Tsuchiaki merely discloses trench capacitors formed in bulk silicon 200 and separated by shallow trench isolation regions 201 (Tsuchiaki at col. 13, lines 26-50; Figure 6(b)). In other words, Tsuchiaki does not teach or suggest a "hybrid" SOI and bulk silicon substrate, let alone a hybrid substrate having the novel features of the claimed invention.

Therefore, Applicant submits that Tsuchiaki, like Witek and Chen, does not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

In summary, Applicant submits that the Examiner seriously misunderstands the novel and advantageous features of the claimed device. The Examiner states, for example, that the "processing limitations" recited in the claims do not carry patentable weight ... because distinct structure is not necessarily produced". However, the Examiner is completely and utterly incorrect. Specifically, conventional processes do not result in a completely buried insulator layer (e.g. 102, Figure 1D) where the insulator layer is completely surrounded with crystallized silicon. This is an important feature of the "hybrid" substrate because it helps to allow a first device in a SOI region to be formed near a second device which is accessing bulk

silicon. Instead, conventional devices merely form the insulator layer and form another silicon layer thereon. Therefore, instead of resulting in the structure of the claimed invention, for example, in Figure 1C, conventional processes result in a structure similar to that illustrated in Chen at Figure 1, where the insulator layer 14 is not completely surrounded with the substrate material. Note for example, that in Chen, the insulator layer runs the length of the substrate and therefore, a device could not access bulk silicon in the Chen device.

In addition, as shown in the Application at Figure 1D, the resulting structure of the claimed invention allows devices formed in the SOI region to be completely isolated from other devices. Note, for instance that a device can be formed on one of the silicon islands between the oxides 104 and be completely isolated from a device on another silicon island. This is completely different, for example, than the Chen device in which the isolation oxide 38 does not completely isolate the left and right device (Chen at Figure 1). Therefore, clearly the processes in the claimed invention result in a wholly different and advantageous structure compared to the prior art devices.

Further, the Examiner alleges that there is insufficient disclosure in the Specification to enable one skilled in the art to make and/or use the device with respect to the use of a SiGe epitaxial process. Applicant respectfully disagrees and submits that the Specification completely and unambiguously explains, for example, how SiGe epitaxial process can be used to form the claimed device.

For example, the Application spends many pages explaining the process of forming the claimed device. In particular, the Application refers to Figure 4B and states that "an epitaxial lateral overgrowth is performed in a manner known in the art" (Application at page 13, lines 11-13). Referring to Figure 5, the Application also explains the process for forming the device in Figure 4B stating that "through step 502B ... by an epitaxial lateral overgrowth process in which a single crystal silicon can be formed on top of the dielectric film by lateral overgrowth from the exposed Si substrate" (Application at page 14, lines 6-9). Further, the Application clearly provides that "the invention could be modified to implement a SiGe epitaxial process to form islands with SiGe, or other III-V compounds, to mix silicon with other semiconductor or conductive materials on an insulator" (Application at page 16, lines 10-12). Applicant submits that any person of ordinary skill in the art would understand the

process of the claimed invention and would clearly and easily how SiGe or any other III-V compound may be used instead of silicon, to form the claimed device.

Therefore, Applicant respectfully submits that the claimed device is clearly and completely explained in the Application and that none of the references teach or suggest the claimed invention.

III. FORMAL MATTERS AND CONCLUSION

The Examiner objects to the Brief Description of the Drawings in the Specification, alleging that Figures 1B-1D, 2D-2E, and 4B-4C are not mentioned. Applicant notes, however, that the Brief Description of the Drawings clearly describes "1A-1E", "2A-2F" and "4A-4D", and submits that this is a customary and acceptable method of describing the drawings.

In view of the foregoing, Applicant submits that claims 24-28, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

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